Customer No.: 31561
Docket No.: 12919-US-PA
Application No.: 10/709,467

AMENDMENT

To the Specification:

Please replace the paragraph [0007] with the following replacement paragraph.

[0007] FIG. 1 is the block diagram of the source driver f the traditional TFT LCD device. The TFT LCD device uses the source driver and the gate driver to drive the pixels. The color correction data are sent to the source driver to correct the displayed color. The source driver as shown in FIG. 1 generally includes the shift register 100, the line latch 102, the level shifter 104, the digital to analog converter (DAC) 106, the output buffer 108, the signal receiver 110, and the data register 112. The DAC 106 receives the voltage levels VGMA1-VGMA14 of the parallel inputted gamma correction curves. The signal receiver 110 receives the input signal D00P, D00N, D01P, D01N, D22P, and D22N such as RSDS related signals. The output buffer 108 outputs the signals Y1, Y2, to drive the pixels to display. DATPOL and POL control the polarities of the driving voltages of the pixels. D101 and D102 are horizontal start pulses, SHL is a start pulse, CLK1 is a clock signal, CLKP and CLKN are differential clock signals. The traditional source driver in FIG. 1 is well known to one skilled in the art and not further described here.